Lab Introduction

Matthew Worcester (BNL)
for the CE design and testing team

Cold Electronics Mini Summer School
7/18/16

Lab Safety

If you are participating in our Lab practicals or attending the demos Tuesday afternoon:

1. Read the ESR
2. Listen to my overview of Cryogen safety
3. Sign the acknowledgement sheet

Cryogen Safety

- Only people who have taken the BNL Cryogen Safety training may handle cryogenic material or move dewars containing cryogens
- If you want to handle cryogenic materials, log in with your BNL ID (if you have one) and select Cryogen Safety (and don't flunk the course):

  https://www.bnl.gov/training/pass/

- Everyone handling cryogenic material must wear: facemask, insulated gloves, long sleeves and pants, closed-toed shoes
- Everyone watching the demo must wear: safety glasses, long pants, closed-toed shoes
- Emergency response: in case of serious burn or oxygen-deficient atmosphere from cryogenic materials, call x2222 or x911

Lab 1-216

- Joint SBND/DUNE testing lab for cold electronics
- Goal: validate all cold electronics for SBND and ProtoDUNE
  - Everything tested here before shipping to CERN or FNAL
- Develop teststands and test procedures for:
  - FE and ADC ASICs
  - Front end motherboards (FEMB)
  - Cryostat feed-through and warm electronics
- Joint effort between BNL and several other institutions

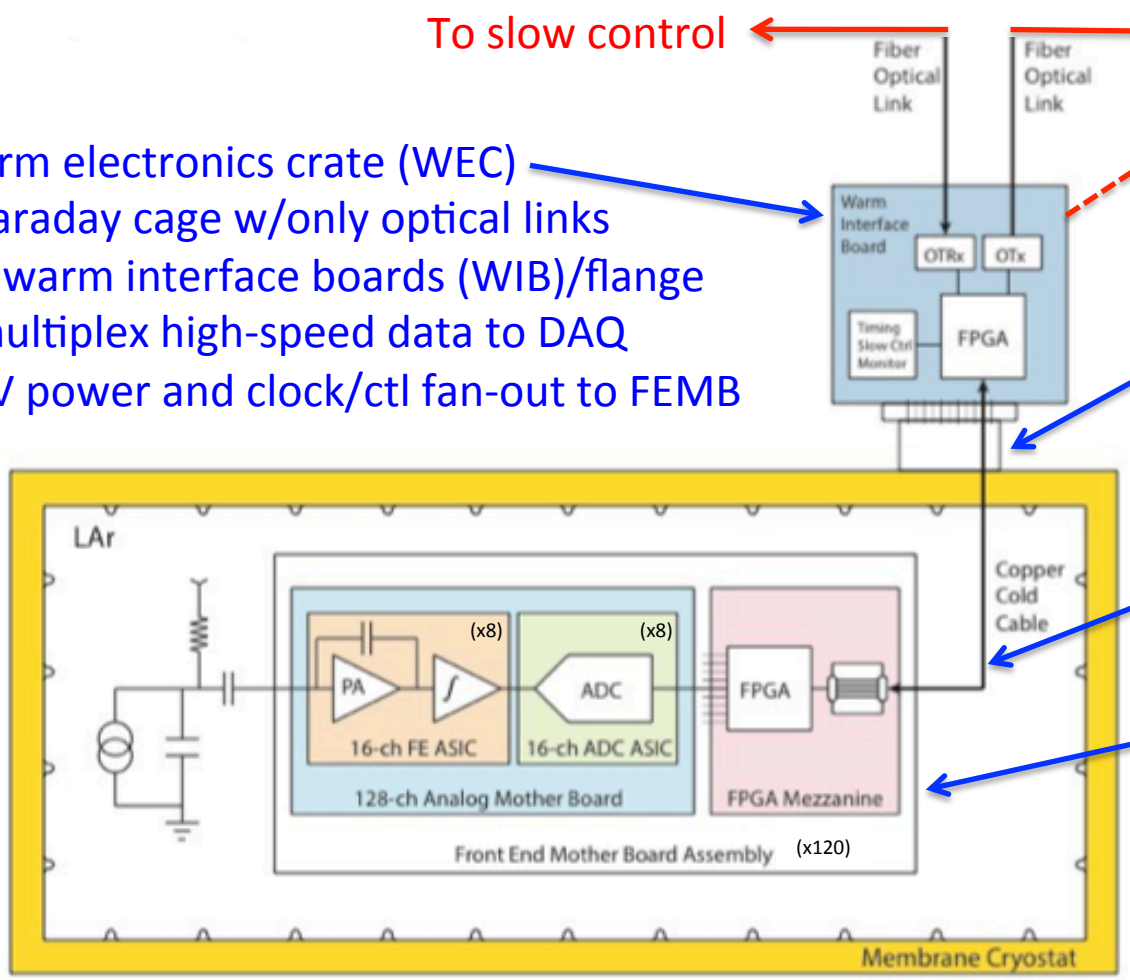
TPC Cold Electronics

To slow control

To DAQ (RCE/FELIX)

Real-time diagnostic readout via Gig-E

Warm electronics crate (WEC)
- Faraday cage w/only optical links
- 5 warm interface boards (WIB)/flange
- multiplex high-speed data to DAQ
- LV power and clock/ctl fan-out to FEMB



Cryostat feed-through (x6)
- warm flange
- 20 FEMB (1 APA)/flange

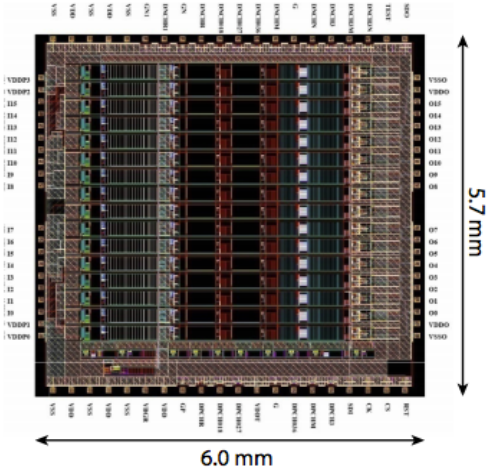
Cold cable (x120)
- Samtec 26 AWG Cu twin-ax

Front-end Mother Board (FEMB) x120 (20/APA)
- FE charge amplifier with programmable gain/shaping for each channel
- 12-bit ADC at 2 MS/sec
- 4 x 1.28 Gbps links

What are all these things?

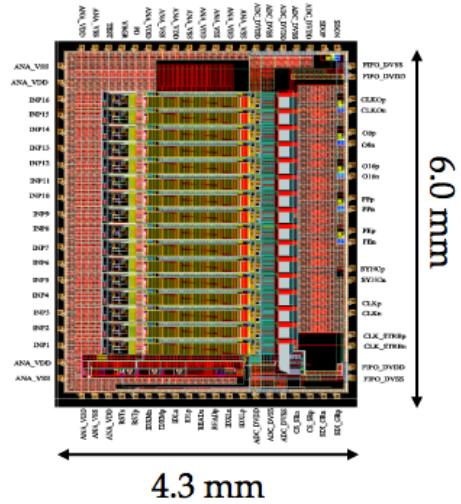
- Front-end (FE) and ADC ASICs
- FEMBs
- Cryostat feed-through and flange
- Warm Interface Board (WIB)
- Power and Timing Card (PTC) and backplane

Cold ASICs



FE

- 16 programmable channels
- Charge amplifier, filter
- Adjustable gain
  - 4.7, 7.8, 14, 25 mV/fC
- Adjustable filter time constant
  - 0.5, 1, 2, 3 µsec peaking time
- Selectable collection/non-collection wire mode
  - 200/900 mV baseline

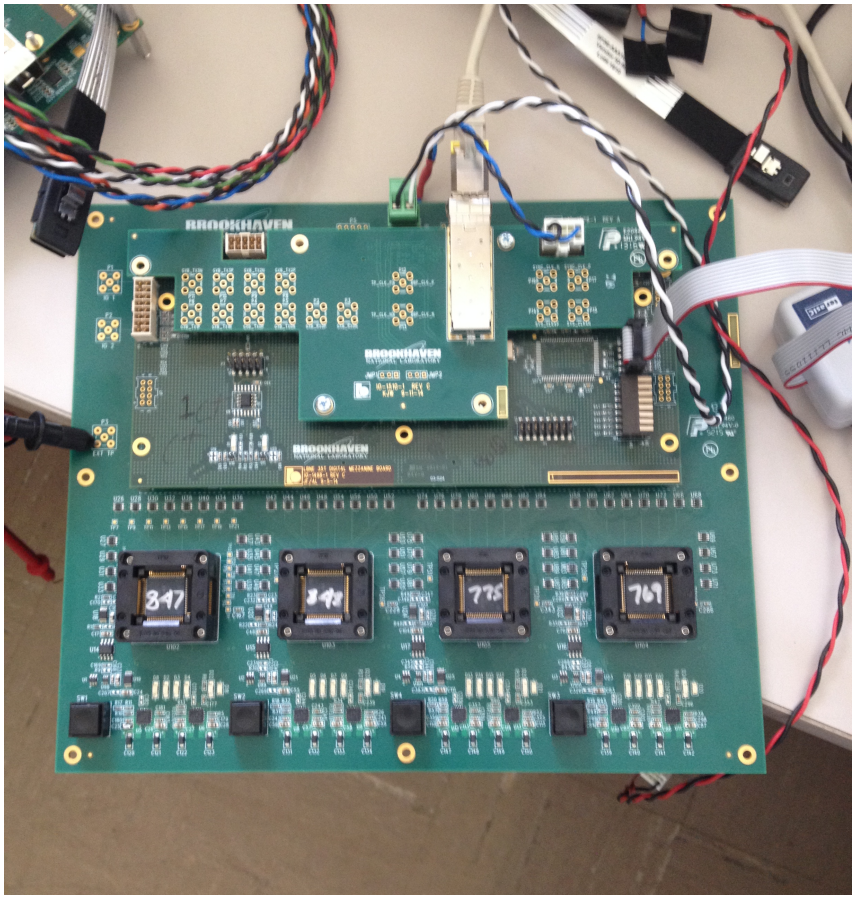


ADC

- 16 programmable channels
- 12-bit ADC sampling at 2 MHz
- ADC “stuck codes” issue in 35ton simulated and solved in next revision
  - External review Apr 7-8 was very positive
  - Expected to be sent out for MPW production by end of the month

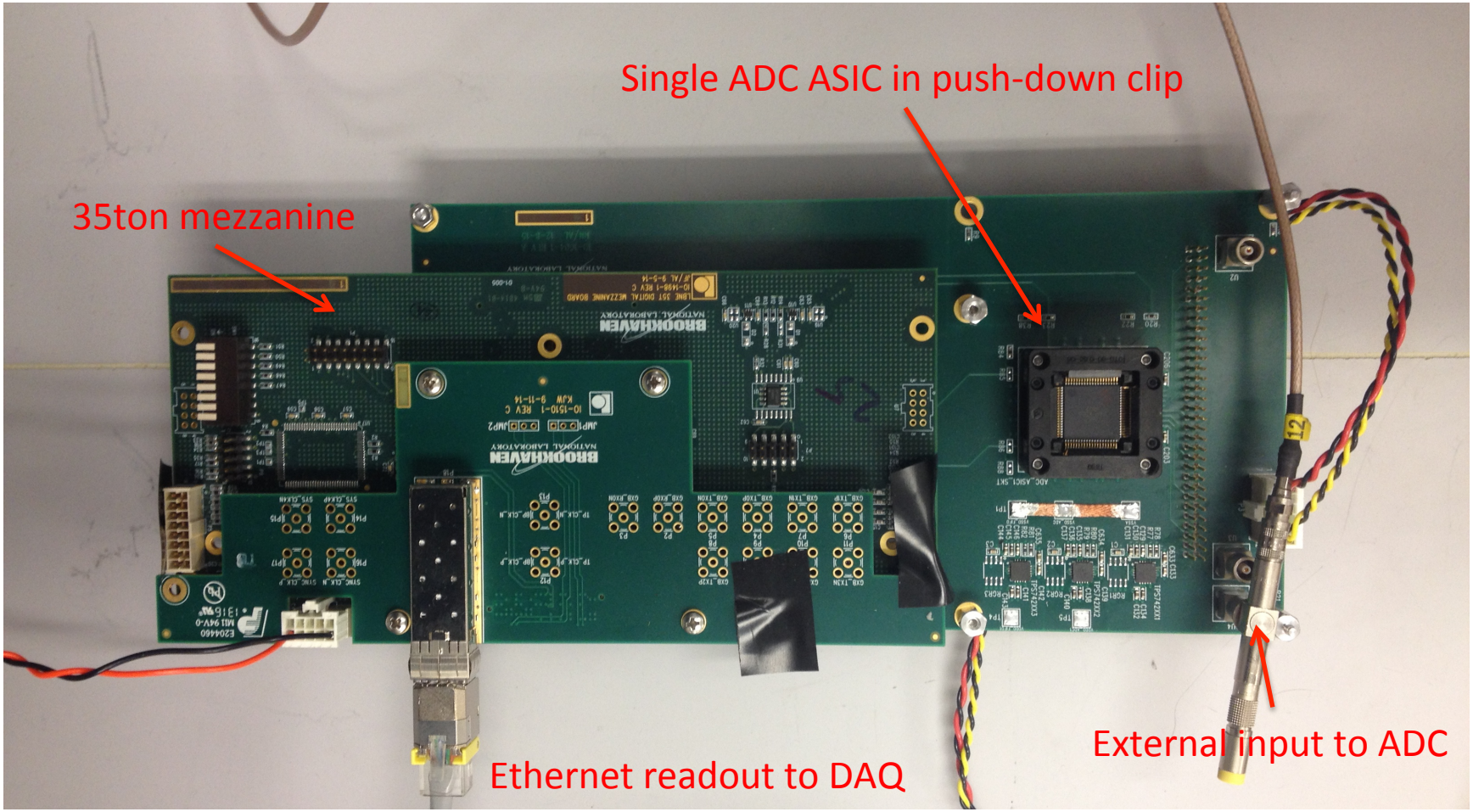
FE ASIC Testboard

- Prototype FE ASIC test board
  - Controlled by 35ton FPGA mezzanine
  - External DAC
  - 14-bit ADCs
- Readout each FE ASIC on all settings
  - Gain, shaping time, baseline
  - Also use internal pulser on current P1 version of FE ASICs

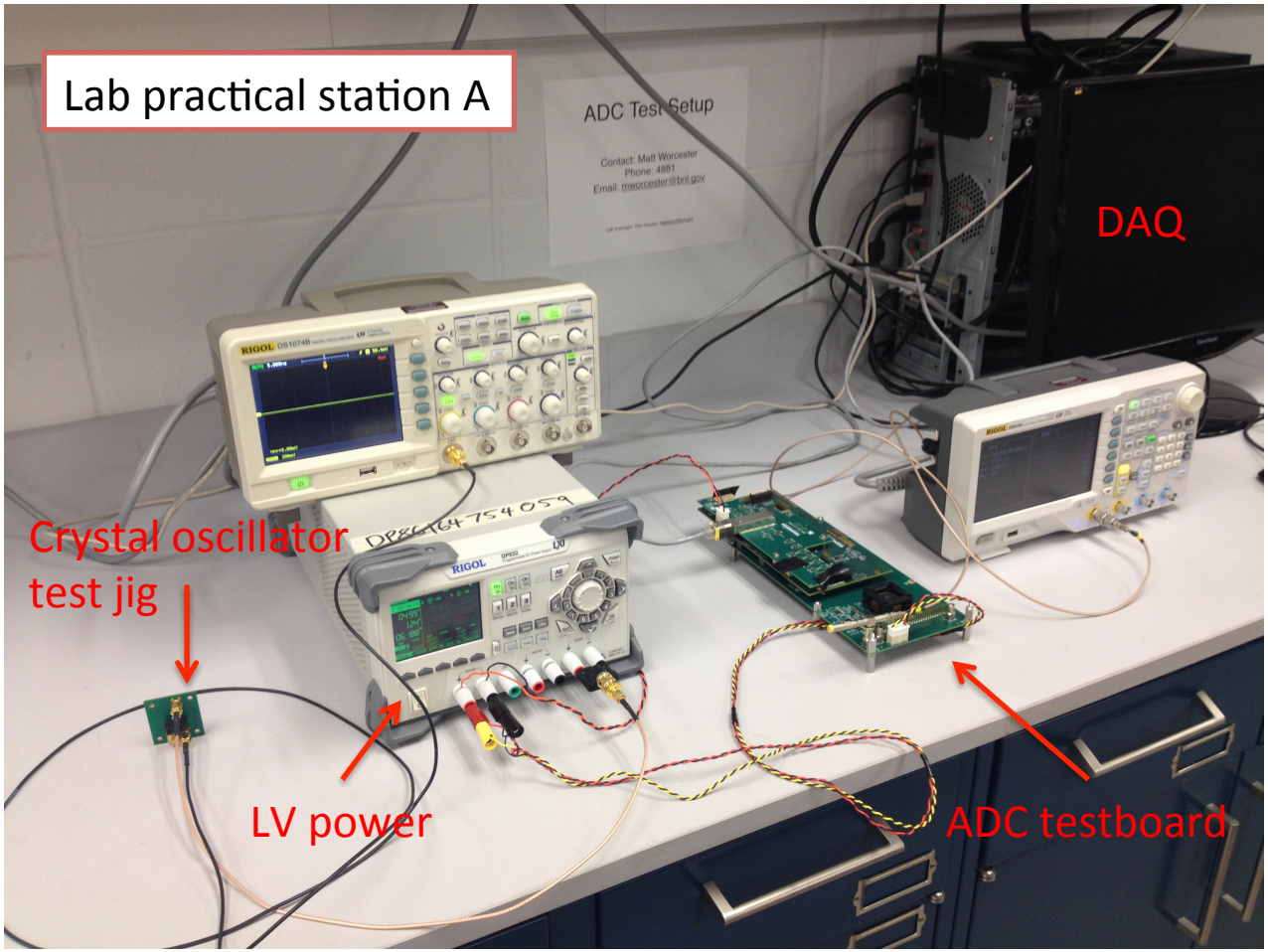


4 FE ASICs in push-down holding clips

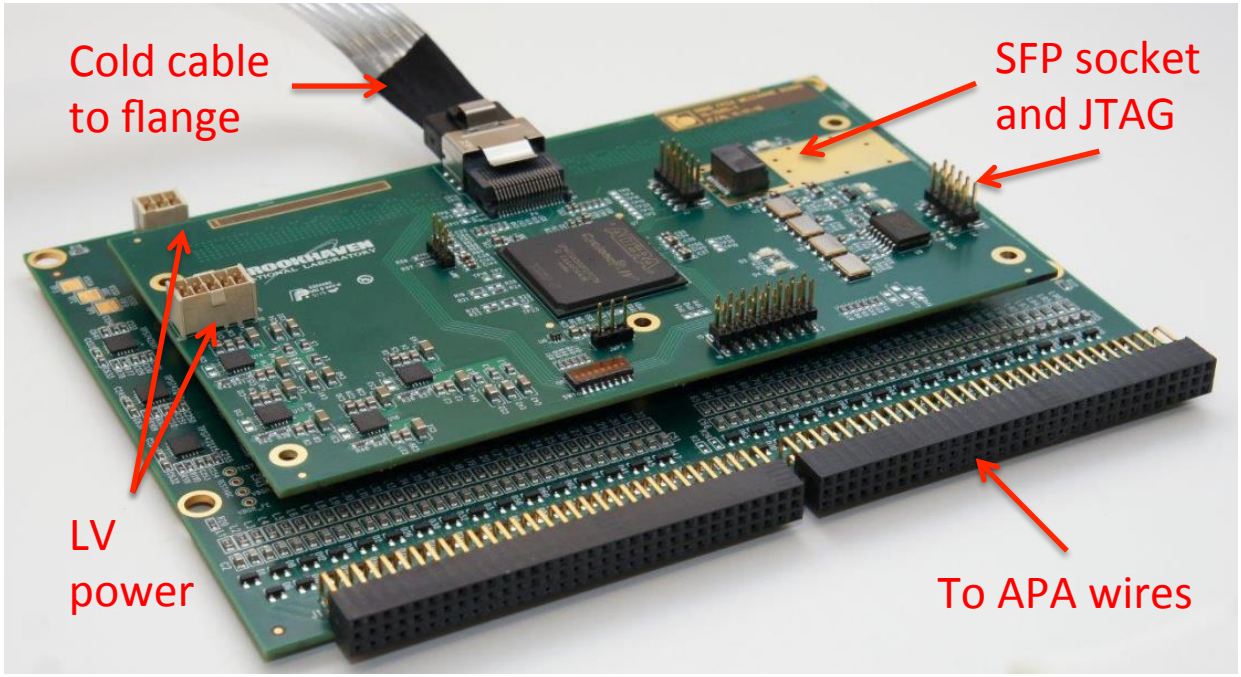
ADC ASIC Testboard

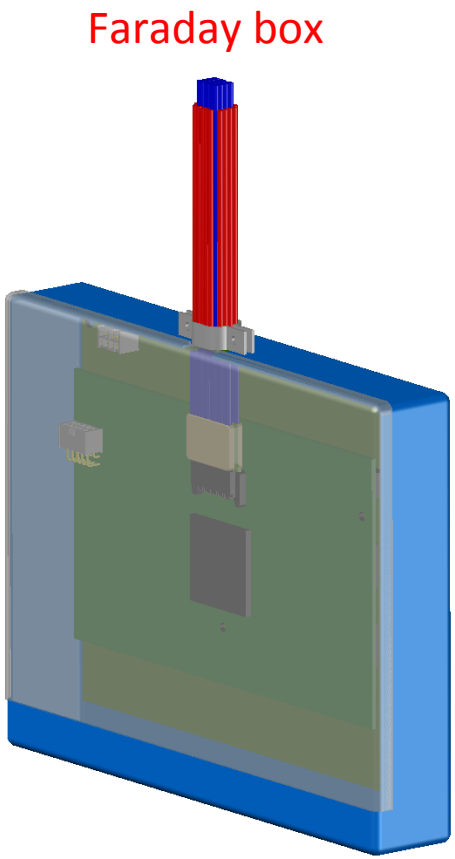


ADC ASIC Teststand



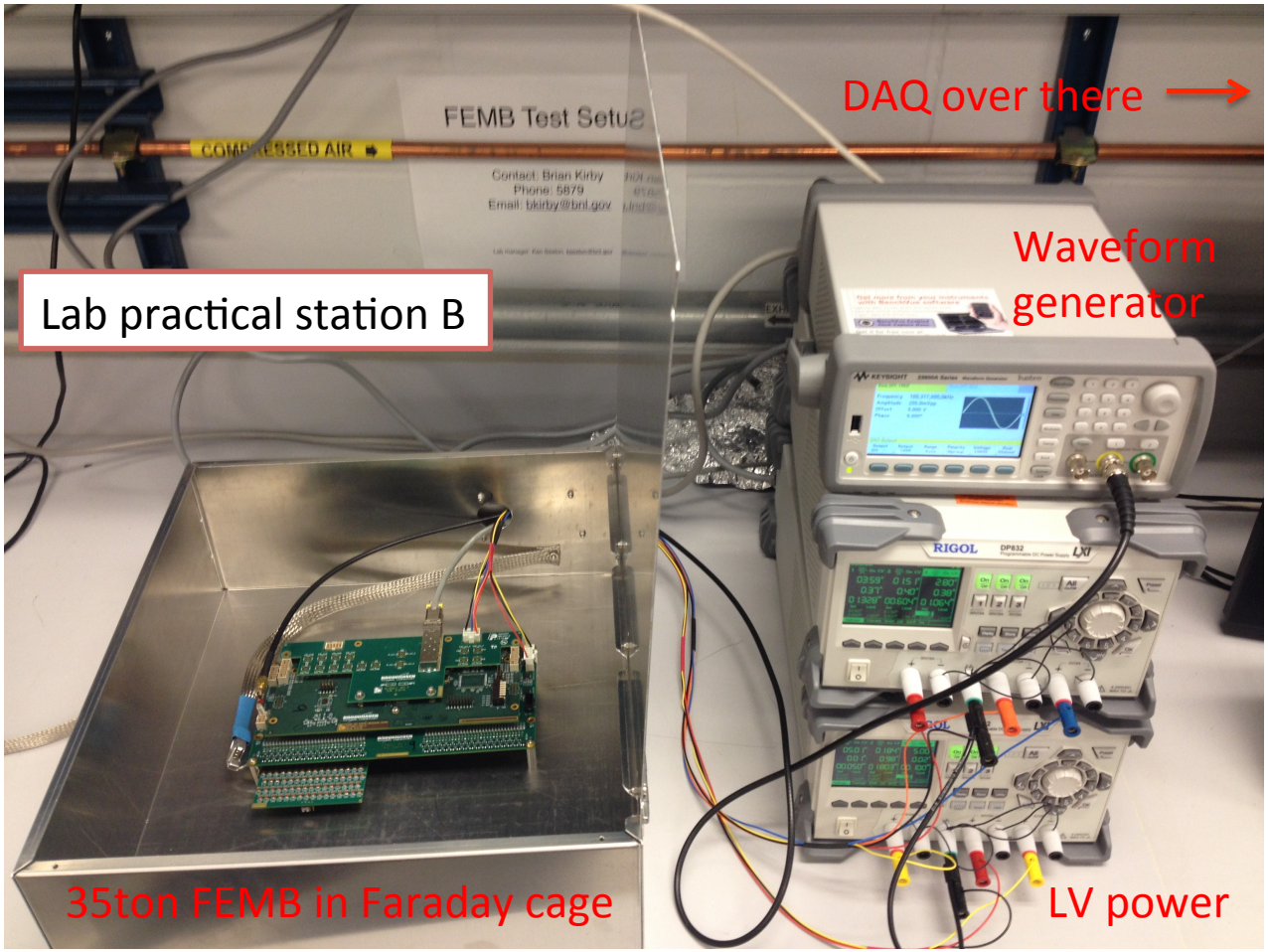
FEMB



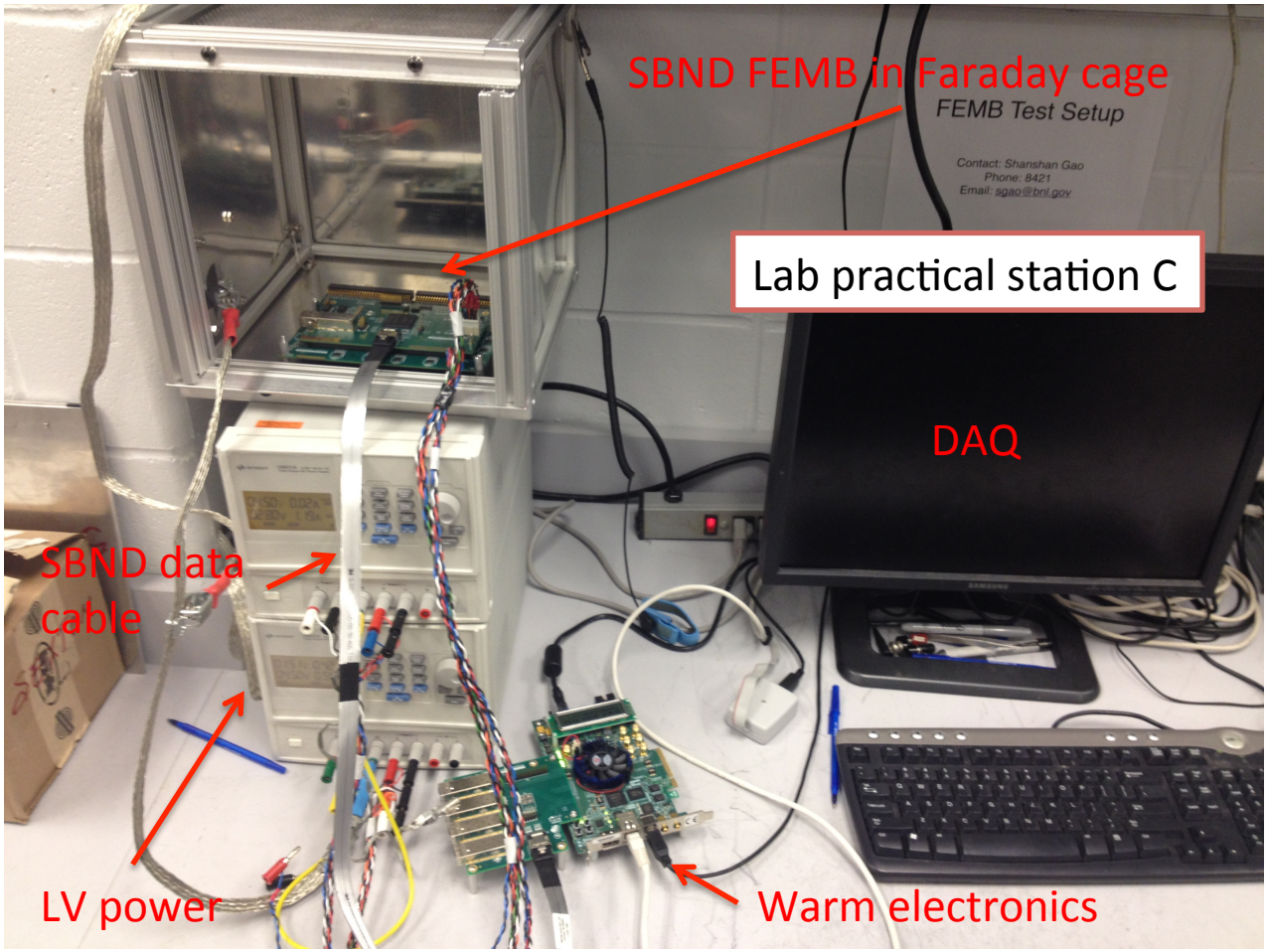


- 128 channels of digitized TPC wire readout
  - 8 FE ASICs/8 ADC ASICs on the analog motherboard
  - Controlled by 2 COLDATA/1 FPGA on the mezzanine
- Mounted in modular Faraday box with built-in cable strain relief

35ton FEMB Teststand

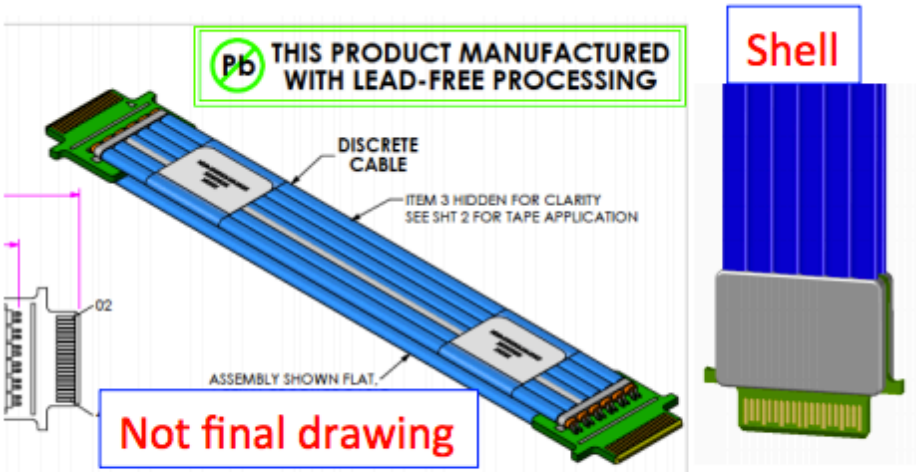


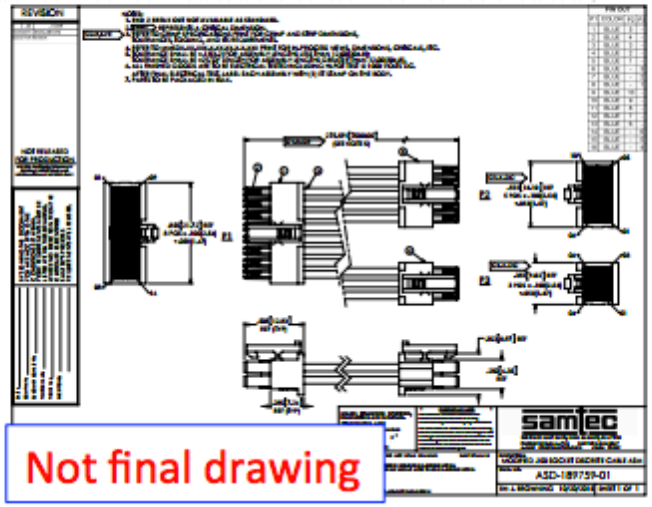
SBND FEMB Teststand



Demo in cryo at 4:15 pm Tuesday afternoon

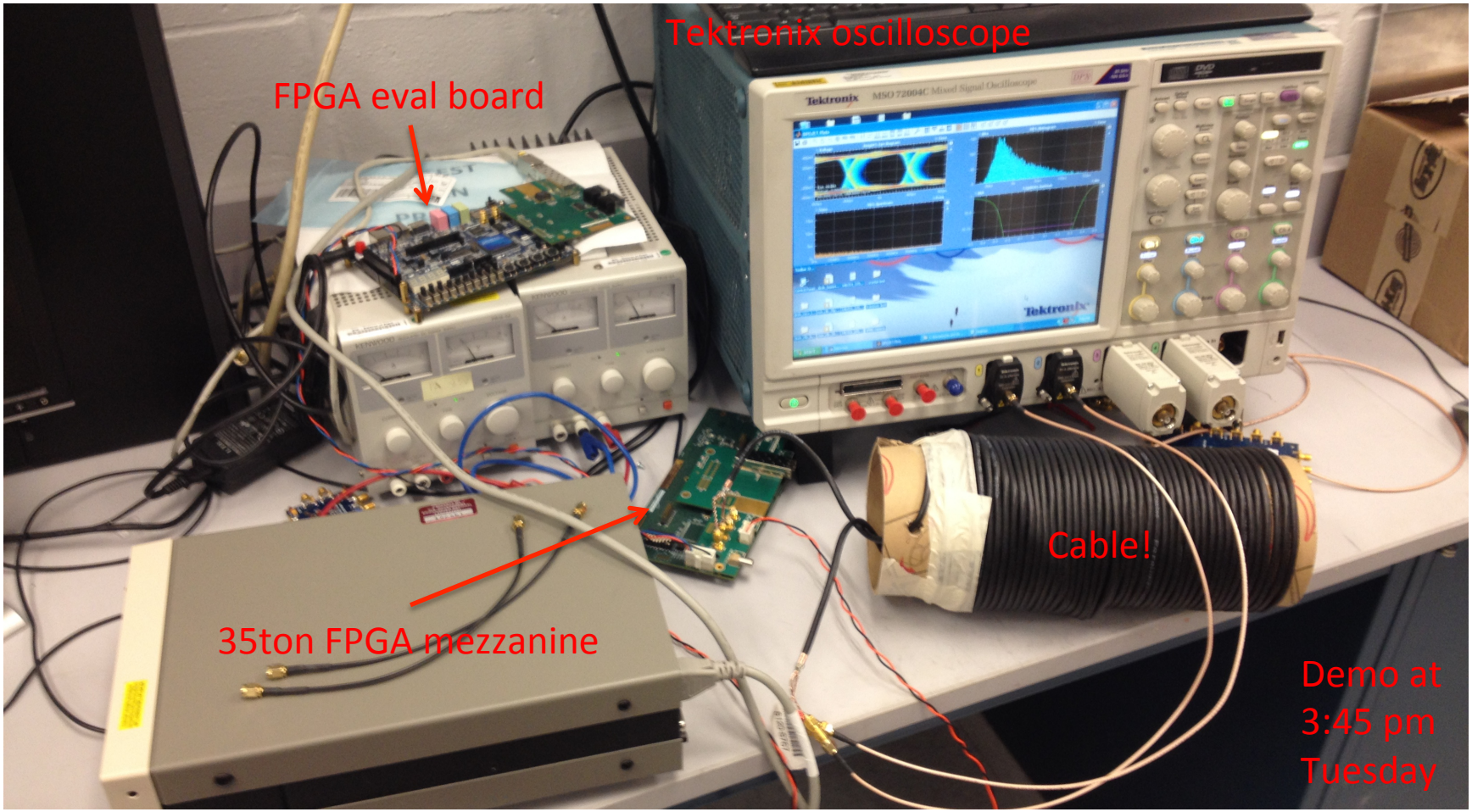
Samtec Cable Bundles



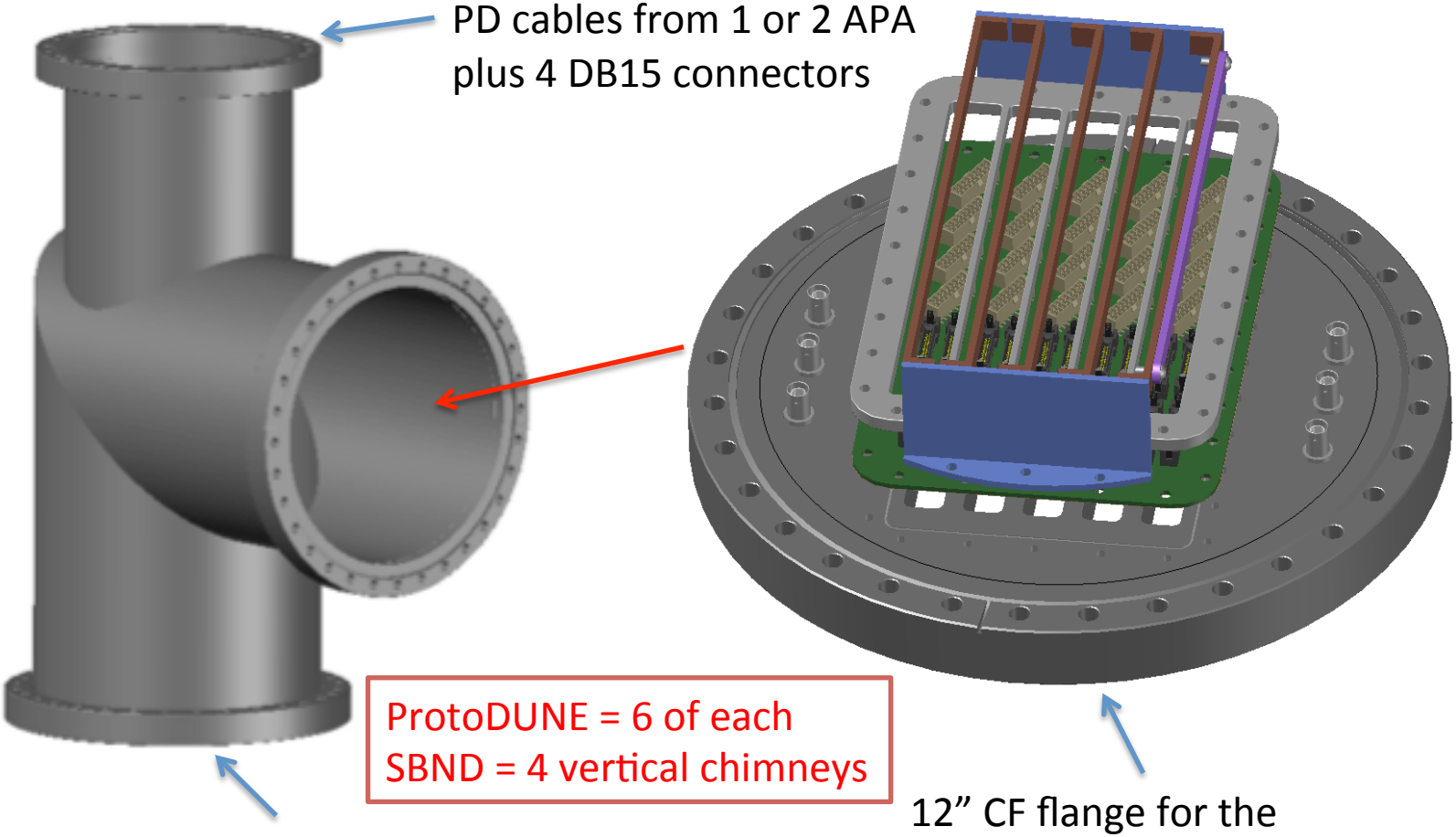


- 4 x 1.2 Gbps high-speed data links from each FEMB to the flange
- Clock, control, and FPGA programming links
- 12 pairs of Samtec 26 AWG copper twin-axial cable with THV insulation
- Samtec HSEC08 connectors to both FEMB and flange

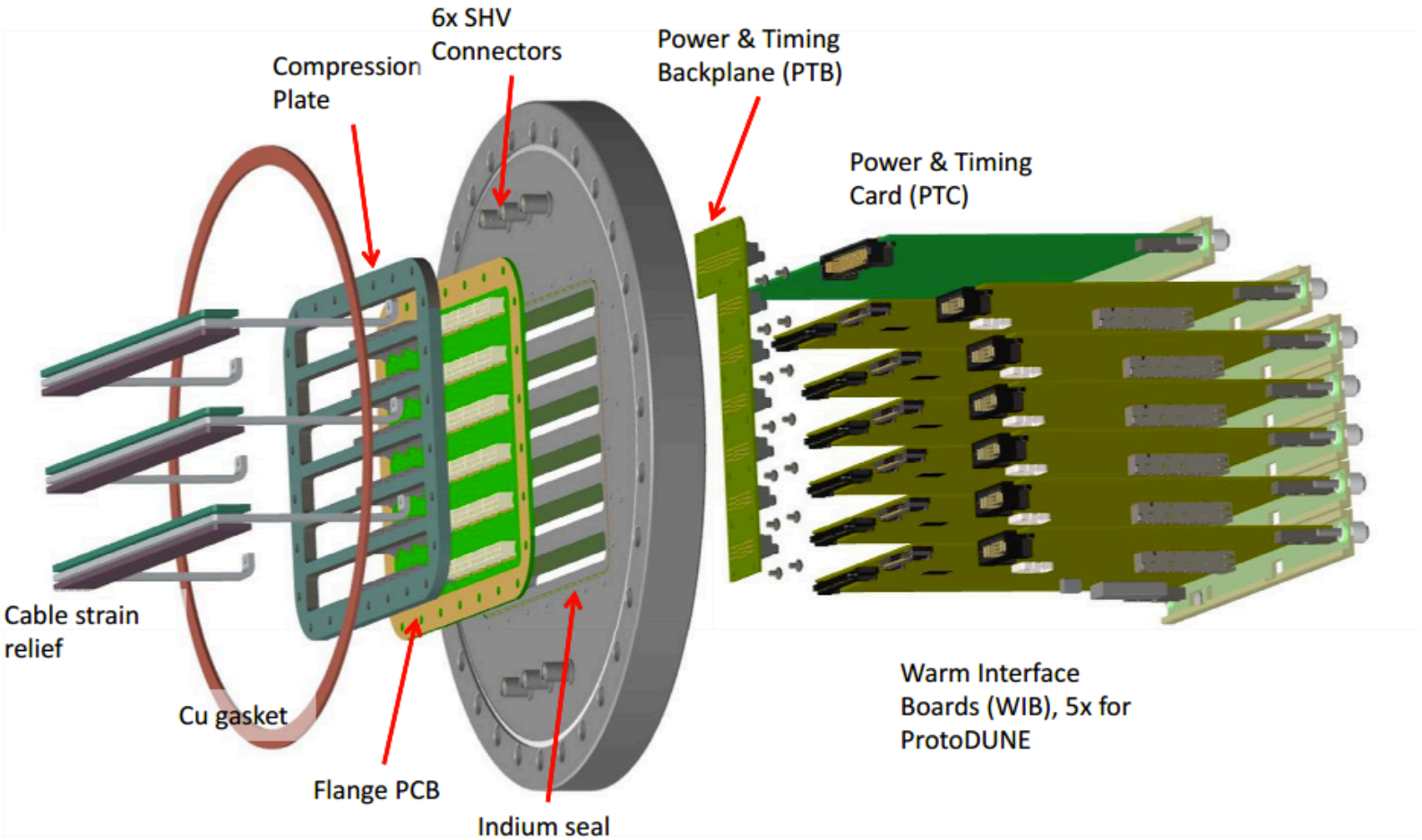
Cable Test Setup



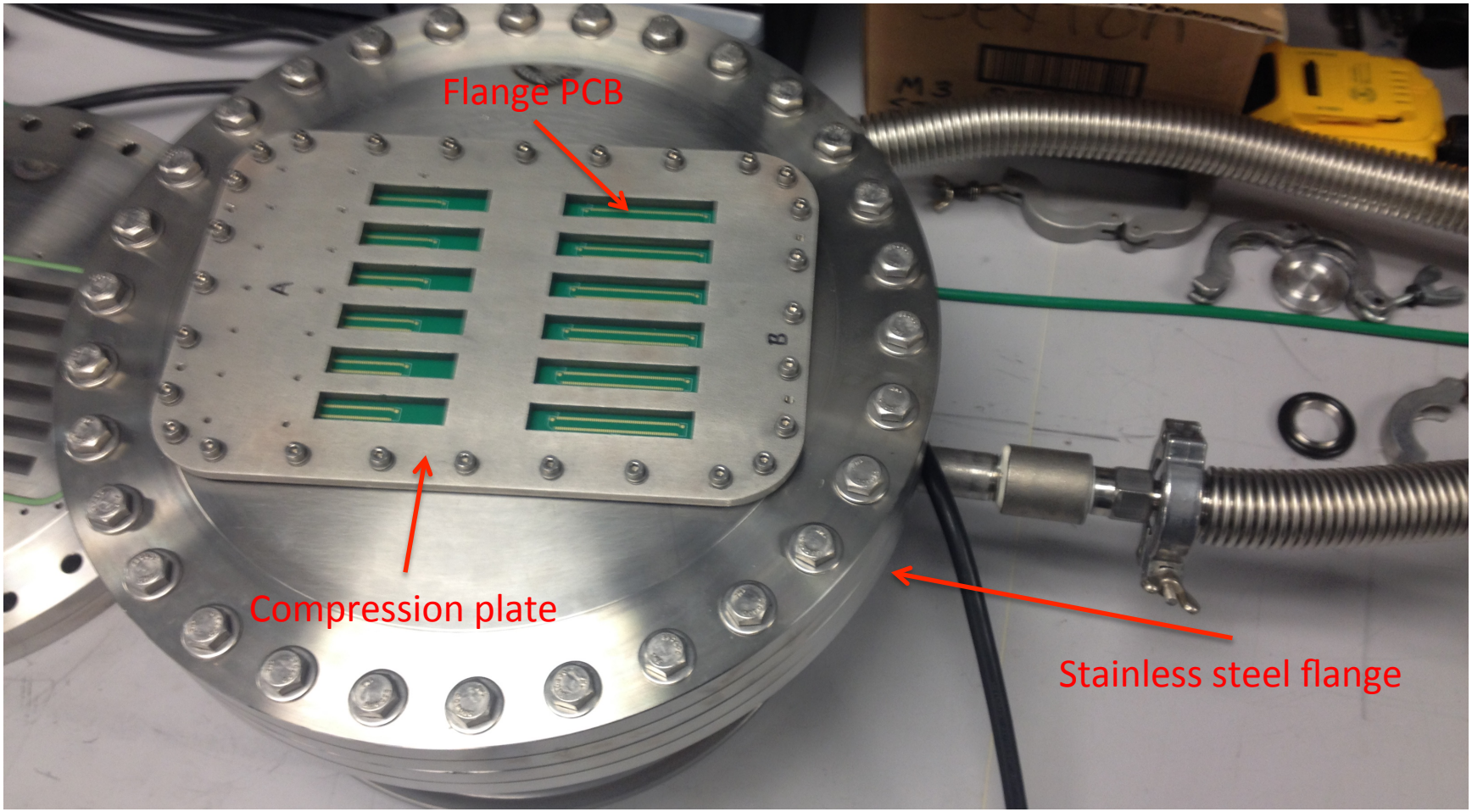
Cryostat Flange and Feed-through



Cold Electronics Flange

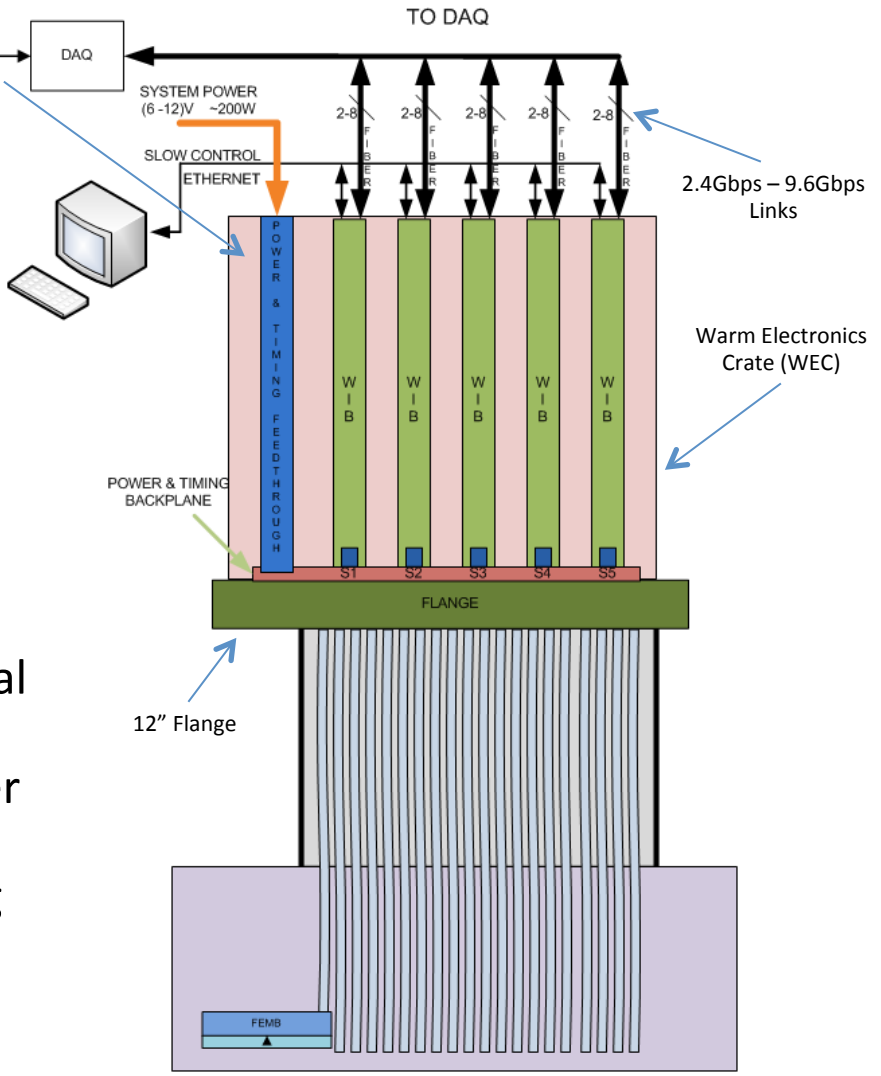


Flange Test Bench



Warm Interface Electronics

- One Warm Electronics Crate (WEC) per flange containing:
  - 5/6 Warm Interface Boards (WIB)
    - Each WIB controls up to 4 FEMBs
  - 1 Power and Timing Backplane (PTB)
  - 1 Power and Timing Card (PTC)
- Installed directly onto flange board
  - Receive high-speed data from cold cable
  - Send data to DAQ over 2-8 fiber optical links per WIB
  - Receive 50 clock and sync/control over fiber links to PTC or WIB
  - Interface to slow control system using fiber GIG-E
  - Manage power and control for FEMBs



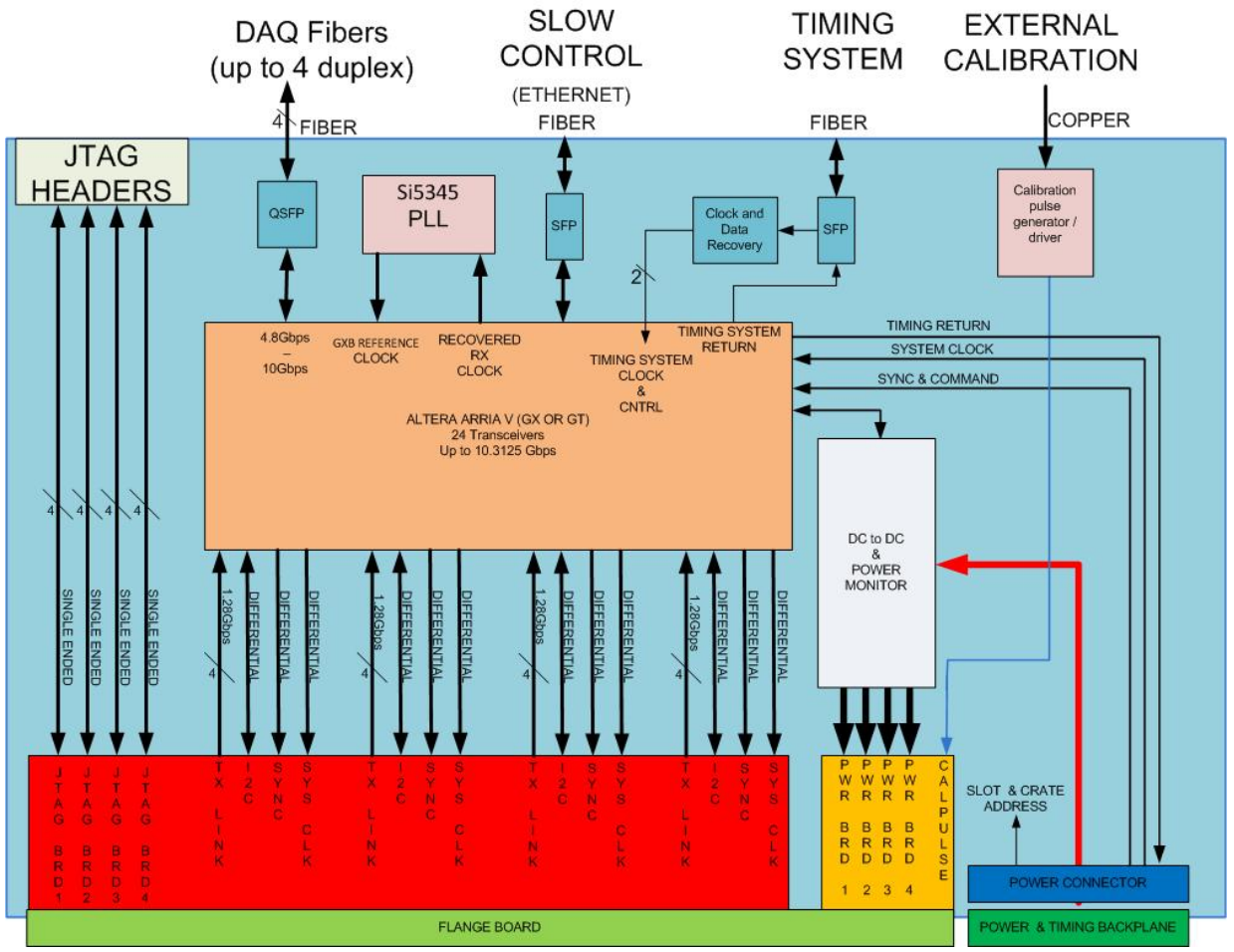
Warm Interface Board

Provides timing/ control and LV power fan-out to FEMB

Each WIB controls up to 4 FEMBs

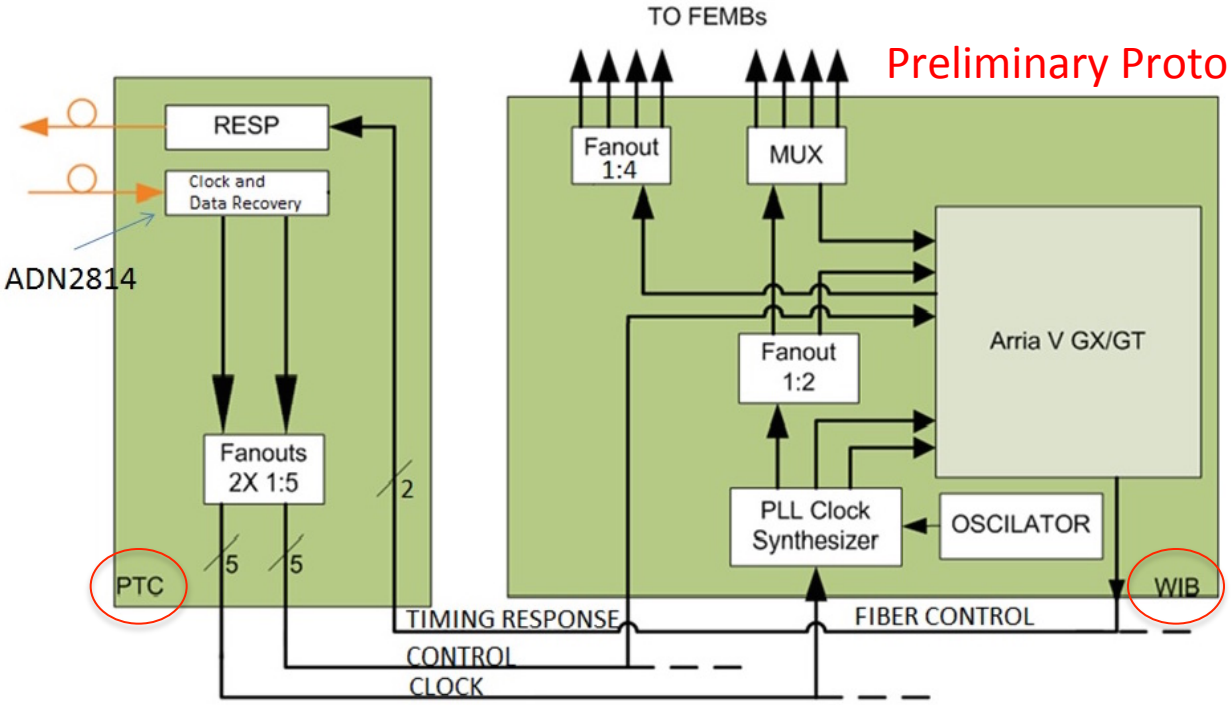
Packages high-speed data to send to DAQ:
- Nevis design for SBND
- SLAC RCEs for ProtoDUNE

Stand alone readout over GIG-E for integration testing and local diagnostics



Preliminary ProtoDUNE design

Power and Timing Card



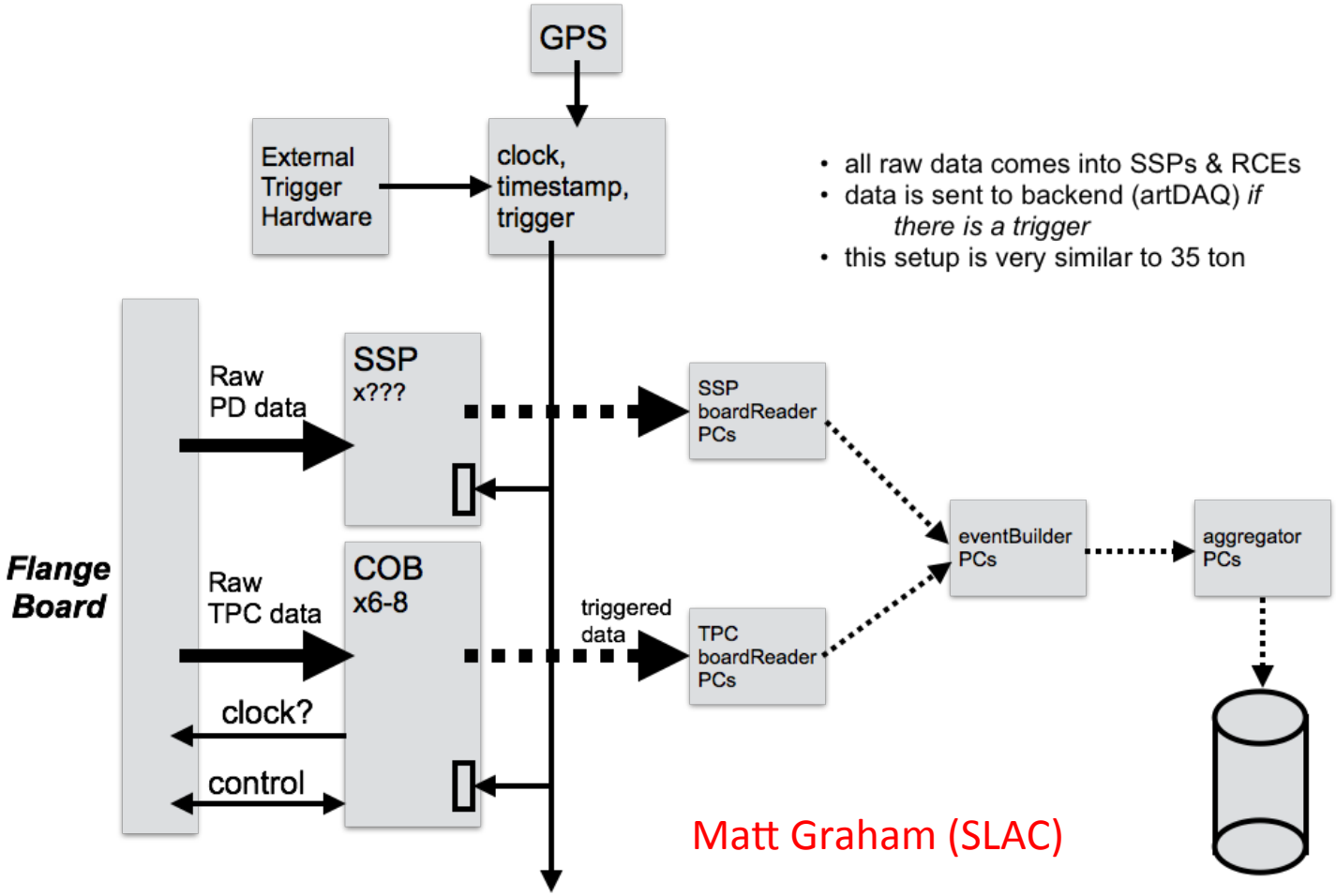
- ProtoDUNE design receives LV power and encoded system clock/control and fans out to the WIBs; returns link for synchronization check
- SBND design is simple fan-out of clock and LV power with no return

Integration Teststand

- Full CE readout chain through the warm electronics
  - Use prototype FEMBs
  - Dewar and other cryogenic infrastructure
  - Test warm components
    - Flange
    - Warm interface electronics
    - Cable and connectors
- Goal: full validation of CE through the warm interface
  - Use GIG-E readout from WIB, not required to have final DAQ

MicroBooNE prototype integration teststand (Hucheng Chen)

ProtoDUNE DAQ



Lab Practical Stations

A. ADC test setup
B. 35ton FEMB test setup
C. SBND FEMB test setup

These are prototype test setups, running prototype test boards and FEMBs.

Development of final (more sophisticated) test stand software and procedures will take place over the coming months. We expect many of you will take leading roles in developing the tools for final tests of pre-production and production components for ProtoDUNE & SBND.

Lab Practical Teams

- Team 1
  - Jonathan, Joe, Raquel, Wenbin, Wei, Yue
  - Schedule: practical #1 at station A, #2 at B, #3 at C
- Team 2
  - Bill, Jacob, Shannon, Justin, Eric, Jian, Kevin
  - Schedule: practical #1 at station B, #2 at C, #3 at A
- Team 3
  - Mary, Robert, David, Steve, Xiaoyue, Dean, Zach
  - Schedule: practical #1 at station C, #2 at A, #3 at B

Practical #1: Monday 14:30
Practical #2: Monday 16:00
Practical #3: Tuesday 14:30

If you haven't registered but want to participate, glom on to a team!

Let's head over to Physics!

(but first we're going over to Bo's lab down the hall)